AMENDMENTS TO THE CLAIMS

Claim 1 (Previously Presented): A method of determining in which of n intervals a sum of two or more numbers resides comprising:

determining the two or more numbers; and

providing fewer than n compress circuits where n is the number of intervals and each compress circuit is adapted to:

input the two or more numbers;

input range information regarding ranges used to define the n intervals; and

compress the two or more numbers and the range information into two or more outputs; and

employing the fewer than n compress circuits to determine in which of the n intervals the sum of the two or more numbers resides,

wherein a result of a floating point computation in a processor is determined based on the determination of which of the n intervals the sum of the two or more numbers resides.

Claim 2 (Previously Presented): The method of claim 1 wherein the two or more numbers are related to an exponent of a first floating point number and an exponent of a second floating point number.

Claim 3 (Original): The method of claim 2 wherein the two or more numbers are related to an exponent of a floating point addend and an exponent of a floating point product.

Claim 4 (Original): The method of claim 1 wherein:

n is greater than 2; and

providing fewer than n compress circuits comprises providing 2 compress circuits.

Claim 5 (Original): The method of claim 4 wherein each compress circuit comprises adder logic.

Claim 6 (Original): The method of claim 4 wherein each compress circuit is adapted to generate a carry vector and a sum vector based on three inputs.

Claim 7 (Original): The method of claim 1 wherein employing fewer than n compress circuits to determine in which of the n intervals the sum resides comprises:

determining a sign check bit for each interval; and

determining in which interval the sum resides based on the sign check bit for one or more of the intervals.

Claim 8 (Original): The method of claim 1 wherein employing fewer than n compress circuits to determine in which of the n intervals the sum resides comprises:

generating carry and sum bits based on the two or more numbers and range information;

selectively providing the carry and sum bits to a plurality of sign check circuits;

determining a sign check bit for each interval based on the selectively provided bits; and

determining in which interval the sum resides based on the sign check bit for one or more of the intervals.

Claim 9 (Original): The method of claim 8 wherein selectively providing the carry and sum bits to a plurality of sign check circuits comprises:

if a bit j of a range value has a first logic value, providing a corresponding bit of a first carry and a corresponding bit of a first sum of a first of the compress

circuits to a first of the sign check circuits that corresponds to the range value; and

if the bit j of the range value has a second logic value, providing a corresponding bit of a second carry and a corresponding bit of a second sum of a second of the compress circuits to the first sign check circuit.

Claim 10 (Original): The method of claim 8 wherein determining a sign check bit for each interval comprises sharing a sign check circuit between two or more of the intervals.

Claim 11 (Previously Presented): An apparatus for use in determining in which of n intervals a sum of two or more numbers resides comprising:

fewer than n compress circuits where n is the number of intervals and each compress circuit is adapted to :

input the two or more numbers;

input range information regarding ranges used to define the n intervals; and

compress the two or more numbers and the range information into two or more outputs; and

a plurality of sign check circuits coupled to the compress circuits, the sign check circuits adapted to generate a sign check bit that corresponds to each of the n intervals based on the two or more outputs generated by the compress circuits,

wherein a result of a floating point computation in a processor may be determined based on the sign check bits.

Claim 12 (Original): The apparatus of claim 11 wherein the two or more numbers are related to an exponent of a first floating point number and an exponent of a second floating point number.

Claim 13 (Original): The apparatus of claim 11 wherein the two or more numbers comprise an exponent of a floating point addend and an exponent of a floating point product.

Claim 14 (Original): The apparatus of claim 11 wherein:

n is greater than 2; and

the fewer than n compress circuits comprise 2 compress circuits.

Claim 15 (Original): The apparatus of claim 14 wherein each compress circuit comprises adder logic.

Claim 16 (Original): The apparatus of claim 15 wherein each compress circuit is adapted to generate a carry vector and a sum vector based on three inputs.

Claim 17 (Original): The apparatus of claim 11 wherein the two or more outputs of each compress circuit comprise a sum vector and a carry vector each having a plurality of bits.

Claim 18 (Original): The apparatus of claim 17 further comprising a plurality of signal paths adapted to selectively route the bits of the carry and sum vectors of each compress circuit to the plurality of sign check circuits.

Claim 19 (Original): The apparatus of claim 18 wherein the sign check circuits are adapted to determine a sign check bit for each interval based on the selectively routed sum and carry bits.

Claim 20 (Original): The apparatus of claim 18 wherein the plurality of signal paths are configured so as to:

if a bit j of a range value has a first logic value, route a corresponding bit of a first carry and a corresponding bit of a

first sum of a first of the compress circuits to a first of the sign check circuits that corresponds to the range value; and

if the bit j of the range value has a second logic value, route a corresponding bit of a second carry and a corresponding bit of a second sum of a second of the compress circuits to the first sign check circuit.

Claim 21 (Previously Presented): A method of determining in which of n intervals a sum of two or more numbers resides comprising:

determining the two or more numbers; and

providing fewer than n compress circuits where n is the number of intervals and each compress circuit is adapted to:

input the two or more numbers;

input range information regarding ranges used to define the n intervals; and

compress the two or more numbers and the range information into two or more outputs; and

employing the fewer than n compress circuits to determine in which of the n intervals the sum of the two or more numbers resides by:

generating carry and sum bits based on the two or more numbers and range information;

selectively providing the carry and sum bits to a plurality of sign check circuits;

determining a sign check bit for each interval based on the selectively provided bits; and

determining in which interval the sum resides based on the sign check bit for one or more of the intervals,

wherein a result of a floating point computation in a processor is determined based on the determination of in which interval the sum resides.

Claim 22 (Previously Presented): An apparatus for use in determining in which of n intervals a sum of two or more numbers resides comprising:

fewer than n compress circuits where n is the number of intervals and each compress circuit is adapted to:

input the two or more numbers;

input range information regarding ranges used to define the n intervals; and

compress the two or more numbers and the range information into a carry vector and a sum vector;

a plurality of sign check circuits coupled to the compress circuits, the sign check circuits adapted to generate a sign check bit that corresponds to each of the n intervals based on the carry and sum vectors generated by the compress circuits; and

a plurality of signal paths adapted to selectively route bits of the carry and sum vectors of each compress circuit to the plurality of sign check circuits,

wherein a result of a floating point computation in a processor may be determined based on the sign check bits.

Claim 23 (Original): The apparatus of claim 22 wherein the range information comprises a plurality logic 0 bits.

Claim 24 (Original): The apparatus of claim 22 wherein the range information comprises a plurality of logic 1 bits.

Claim 25 (New): The method of claim 1 wherein the providing results in less physical space used than if n compress circuits were provided.